



Sheet 1 of 4

FORM PTO-1449
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
HIT 2 482-06

SERIAL NO.

09/739,758

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2783 2121

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)
H	AA 4,994,982	02/1991	Duranton et al			
H	AB 4,974,169	11/1990	Engel			
H	AC 4,611,299	09/1986	Hori et al			
H	AD 4,777,858	01/1989	Wang et al			
H	AE 4,847,755	07/1989	Morrison et al			
H	AF 4,873,672	10/1989	Etoh et al			
H	AG 4,939,696	07/1990	Katsuo et al			
H	AH 5,010,477	04/1991	Omada et al			
H	AI 5,140,670	08/1992	Chua et al			
H	AJ 5,142,665	08/1992	Bigus			
H	AK 5,239,654	08/1993	Ing-Simmon et al			

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

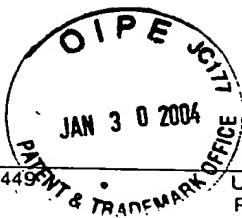
H	AR	Sejnowski et al, "Parallel Networks that Learn to Pronounce English Text", COMPUTER SYSTEMS 1, 1987, pp. 145-168.
H	AS	Asou, "Neural Network Processing", Chapters 2 and 3, Sangyo Tosho pub., pp. 39-68, 69-93 and 118-123.
H	AT	Advanced Micro Devices, MEMORY PRODUCTS DATA BOOK, Jan. 1989, pp. 4-80, 4-81.

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H	AA	5,005,121	04/1991	Nakada et al			
H	AB	5,163,120	11/1992	Childers et al			
H	AC	5,301,340	04/1994	Cook			
H	AD	5,023,833	06/1991	Baum			
H	AE	5,179,680	01/1993	Colwell			
H	AF	5,107,442	04/1992	Weidman			
H	AG	5,165,010	11/1992	Masuda			
H	AH	5,708,836	01/1998	Wilkinson			
H	AI	4,471,426	09/1984	McDonough			
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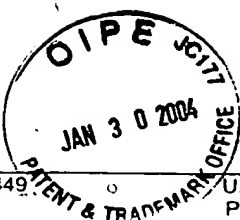
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

H	AR	Eberhardt et al, "Design of Parallel Hardware Neural Network Systems From Customer Analog VLSI 'Building Block' Chips", INTERNATIONAL JOINT CONFERENCE ON NEURAL NETWORKS, June 18-22, 1989, pp. II-183 to II-190.
H	AS	Rumelhart et al, "Learning Representations by Back Propagating Errors", NATURE, Vol. 323, October 9, 1986, pp. 533-536.
H	AT	Nikkei Microdevices, March 1989, pp. 123-129.
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H	AR	Suzuki et al, "A Study of Regular Architectures for Digital Implementation of Neural Networks", 1989 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, May 8-11, 1989, pp. 82-85.
H	AS	Holler et al, "An Electrically Trainable Artificial Network (ETANN) with 10240 'Floating Gate' Synapses", PROCEEDINGS OF THE INTERNATIONAL ANNUAL CONFERENCE ON NEURAL NETWORKS, 1989, pp. 50-55.
H	AT	Manuel, "Are Artificial Neural Networks Finally Ready for Market?", ELECTRONICS, August 1988, pp. 85-88.

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FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. HIT 2 482-06	SERIAL NO. 09/739 758
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U.S. PATENT DOCUMENTS

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AP						<input type="checkbox"/>	<input type="checkbox"/>

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✓	AR	Sawada et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM", PROCEEDINGS IEEE 1988 CUSTOM INTEGRATED CIRCUIT CONFERENCE, pp. 20.3.1 to 20.3.4.
	AS	
	AT	

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